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Power Modeling to Enable System Level Analysis

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POWER MODELING TO ENABLE SYSTEM LEVEL ANALYSIS

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IEEE Std	FDIS	Report on voting
2416 (2019)	91/1867A/FDIS	91/1888/RVD

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IEEE Standard for Power Modeling to Enable System-Level Analysis

Developed by the

Design Automation Committee
of the
IEEE Computer Society

Approved 21 May 2019

IEEE-SA Standards Board

Abstract: In this standard, a parameterized and abstracted power model enabling system, software, and hardware intellectual property (IP)–centric power analysis and optimization are described. Concepts and constructs are defined for the development of parameterized, accurate, efficient, and complete power models for systems and hardware IP blocks usable for system power analysis and optimization. Process, voltage, and temperature (PVT) independence; power and thermal management interface; and workload and architecture parameterization are some of the concepts included.

Keywords: IEEE 2416™, intellectual property (IP) blocks, modeling standards, models, optimization, parameterization, power contributors, power data, process, voltage, and temperature (PVT)

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IEEE Introduction

This introduction is not part of IEEE Std 2416-2019, IEEE Standard for Power Modeling to Enable System-Level Analysis.

All System-on-Chip (SoC) designs today face power issues of one sort or another—maximizing battery life, sizing power grids, controlling leakage power, verifying power sequencing, estimating and modeling power at various abstractions, analyzing electro-thermal effects, and so on.

Despite growing industry and societal concerns with power consumption and significant industry attention, there has not been a standard way of representing power data for use at the system level, especially across a range of process, voltage, and temperature (PVT) points in a single model.

The lack of a complete and robust modeling standard has led to a paucity of power models. Intellectual property (IP) vendors, if they produce any power models at all, produce models that are limited in use and application. As a result, designers and other model users struggle with reliably estimating power during system-level design, ultimately producing SoCs that are less power efficient than they could be. To address this situation, a modeling standard addressing data representation is needed to enable modeling accurate and efficient power and thermal analyses early in the design cycle.

Finally, this standard has incorporated several prior technologies and specifications developed and released by Si2, including *Leakage Power Contributor Modeling*, *Liberty Mode Extensions for Atomic Power Modeling*, *Standards for Efficient System Level Power Analysis*, and *Multi-level Power Modeling*.

Acknowledgments

Grateful acknowledgment is made for permission to use the following source material:

Silicon Integration Initiative, Inc. (Si2™)—*System Level Power Model Interface and Data Representation™, V3.0.*

IEEE Standard for Power Modeling to Enable System-Level Analysis

1. Overview

Even though IEEE Std 1801™-2015[1] added power-state modeling capabilities to the most recently released specification, data representation was not included as that capability was explicitly left out of scope during the IEEE 1801 standardization process. Instead, IEEE Std 1801-2015 assumes another standard will supply the power data to the state-based model defined in IEEE Std 1801-2015. Figure 1 illustrates the power data flow between IEEE Std 1801-2015 and this standard.

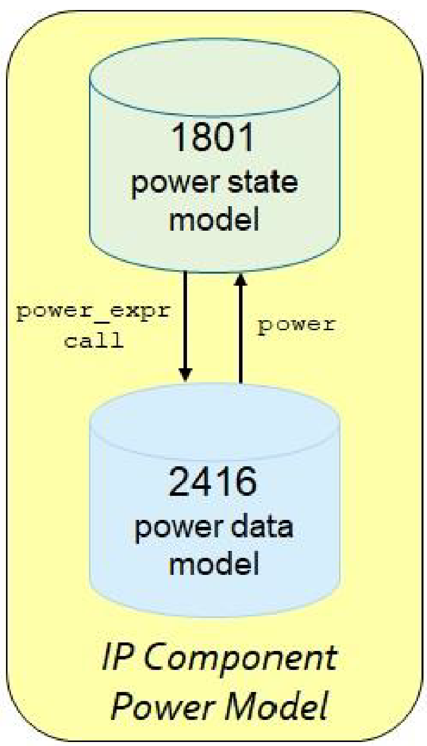

Figure 1—Relationship between this standard and IEEE Std 1801-2015

[1] Information on references can be found in Clause 2.

1.1 Scope

This standard describes a parameterized and abstracted power model enabling system, software, and hardware intellectual property (IP)–centric power analysis and optimization. It defines concepts for the development of parameterized, accurate, efficient, and complete power models for systems and hardware IP blocks usable for system power analysis and optimization. These concepts include, but are not limited to, process, voltage, and temperature (PVT) independence; power and thermal management interface; and workload and architecture parameterization. Such models are suitable for use in software development flows and hardware design flows, as well as for representing both pre–silicon-estimated and post–silicon-measured data. This standard also defines the necessary requirements for the information content of parameterized, accurate, efficient, and complete power models to help guide development and usage of other related power, workload, and functional modeling standards, such as UPF IEEE Std 1801™-2015, SystemC IEEE Std 1666™-2011, and SystemVerilog IEEE Std 1800™-2012. Beyond defining the concepts and related standard requirements, this standard also recommends the use of other relevant design flow standards (e.g., IP-XACT IEEE Std 1685™-2014 [B2][2]), with the objective of enabling more complete and usable power-aware design flows.

1.2 Purpose

This standard supports the ability to develop accurate, efficient, and interoperable power models for complex designs, to be used with a variety of commercial products throughout an electronic system design, analysis, and verification flows.

1.3 Key aspects and considerations

This standard describes a PVT-independent modeling capability that can serve up power data throughout the entire System-on-Chip (SoC) development flow from IEEE 1801 system-level power estimation all the way down to gate-level power calculation. Contributor-based modeling techniques are employed to achieve PVT independence, and multilevel modeling concepts enable a single model to serve various abstraction levels. Contributors are separable, summable components of power consumption that depend on parameters such as transistor widths and stacks, as well as on charging capacitances. Contributors offer the capability to do a “late binding” of specific PVT conditions to an IP model, avoiding the need to characterize the target IP up front under particular PVT conditions.

This standard addresses three separate, but related, modeling concerns: 1) interfaces to other modeling standards, such as IEEE Std 1801-2015, as well as to existing electronic design automation (EDA) tools; 2) persistent data representation and storage; and 3) model evaluation—the conversion of contributor data into energy and power data.

In addition, the following requirements have been identified as being essential to improving both model generation and model usage:

- Direct support for IEEE 1801 IP component power-state model data and interface definitions
- PVT independence: Power data need not be generated at specific PVT points prior to model evaluation
- Ability to coexist with legacy power data formats, such as Liberty [B3]
- Ability to model IP blocks of arbitrary complexity as well as logic primitives, such as `NAND`s, `NOR`s, and Flip-Flops

[2] The numbers in brackets correspond to those of the bibliography in Annex A.

— Ability for a single model to be used in the earliest phases of system design, the latest implementation phases, and all phases in between

The development and standardization of modeling capabilities addressing these issues can provide benefits to both model generators, such as foundries and IP providers, and model consumers, such as IP and SoC architects, SoC verification teams, and energy-aware software developers. For model generators, this development enables efficiency in the model generation and support process (in terms of time, compute resources, and resulting costs). For model consumers, it enables more efficient, reliable, and consistent power analysis and optimization flows from the beginning of the design process to the end. Additionally, the "late binding" of specific PVT conditions provides efficiency benefits for model generators and model consumers alike, including very early stage electrothermal analyses.

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`<Unit name="capacitanceUnit" value="pF" />`

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```
EnergyContributor | Expression | Table | Scalar
```

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Accellera Systems Initiative, "Verilog-AMS Language Reference Manual, Version 2.4.0," May 30, 2014.[3]

IEEE Std 1666™-2011, IEEE Standard for Standard SystemC Language Reference Manual.[4, 5]

IEEE Std 1800™-2012. IEEE Standard for SystemVerilog—Unified Hardware Design, Specification, and Verification Language.

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IEEE Std 1801™-2015, IEEE Standard for Design and Verification of Low-Power Integrated Circuits.

World Wide Web Consortium, "eXtensible Markup Language (XML) 1.0" specification (http://www.w3.org/TR/REC-xml/).[6]

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